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(54) Abstract Title
Maintaining orthogonality between signals

(57) A spread spectrum apparatus for an OQPSK (offset quadrature phase shift keying) DS/CDMA system maintains orthogonality between transmission signals during zero crossing. First and second input signals DI(t), DQ(t) are combined with orthogonal Walsh codes WI(t), WQ(t) and are spread using corresponding PN sequences PI(t) and PQ(t). A zero crossing detector 241 determines whether zero-crossing occurs for both the first and second spread signals XI(t), XQ(t) and outputs a signal to selectors 247, 249 accordingly. First and second delays 243, 245 stagger the spread signals and these signals together with the spread signals XI(t) and XQ(t) are forwarded to the selectors. Ordinarily the first and second spread signals are selected for transmission, but when zero-crossing is detected the staggered versions of these signals are selected to maintain orthogonality. Alternatively only one of the spread signals may be delayed (fig. 8).

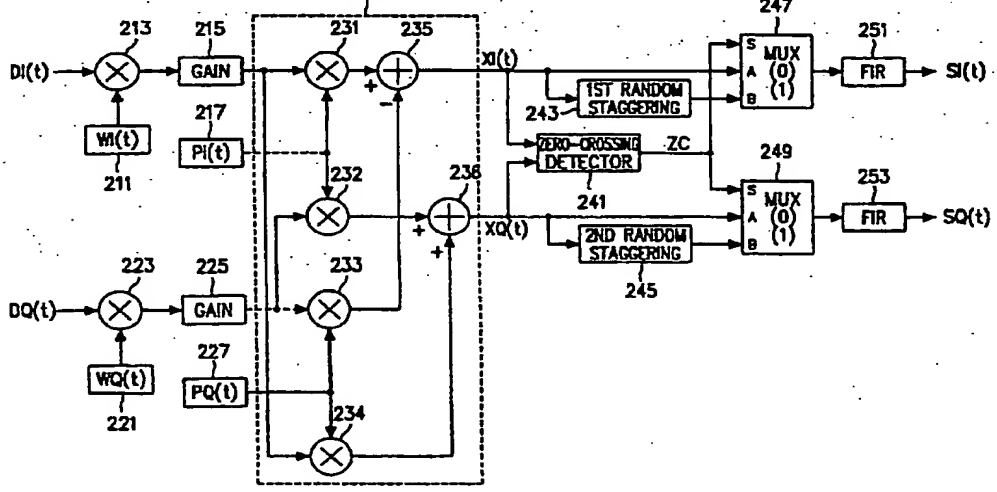

FIG. 2

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

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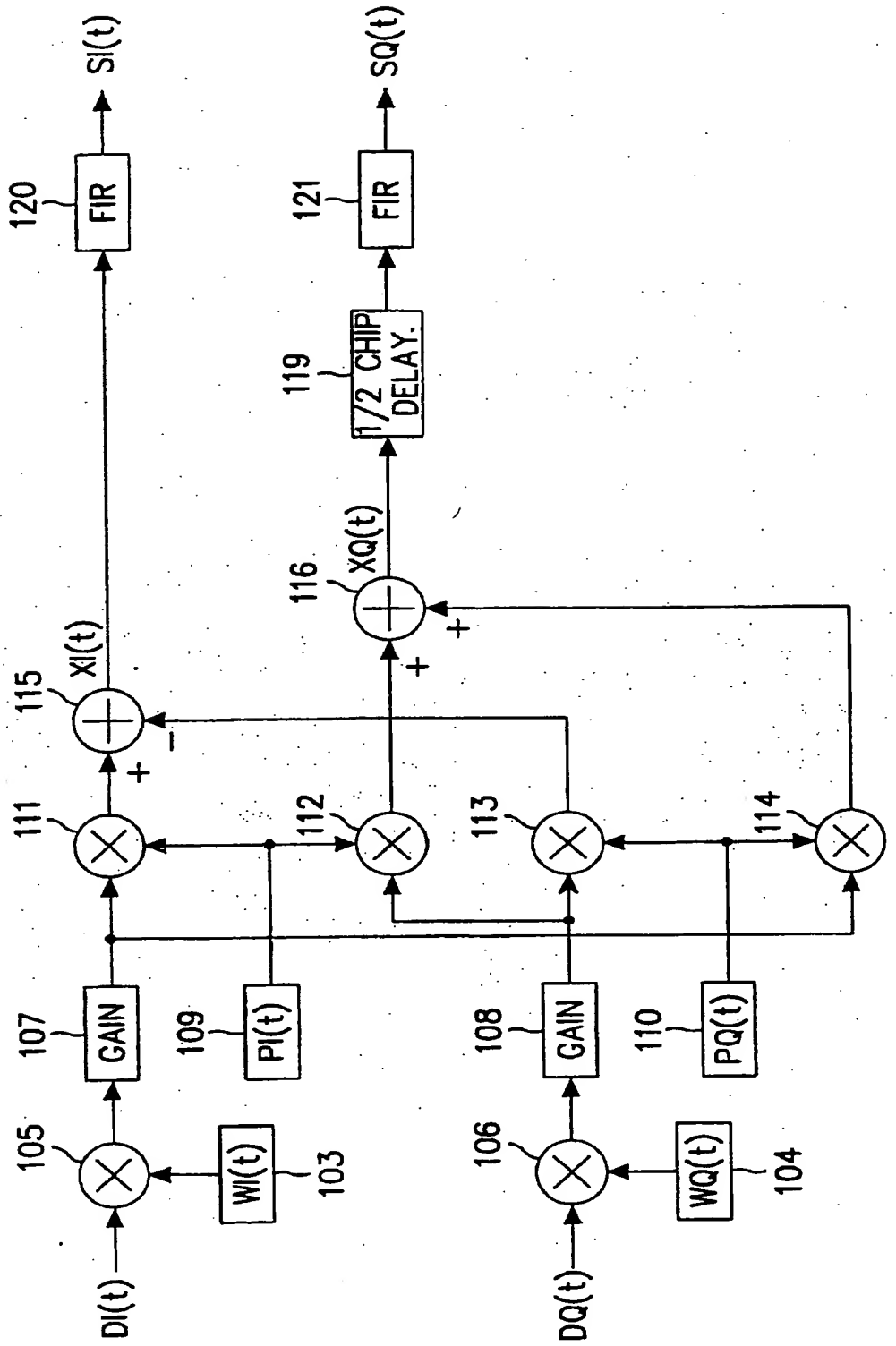
DI(t)
DQ(t)
WI(t)
WQ(t)
PI(t)
PQ(t)
GAIN
GAIN
FIR
FIR
1/2 CHIP DELAY.
XI(t)
XQ(t)
SI(t)
SQ(t)
+
+
+
-
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
119
120
121

FIG. 1

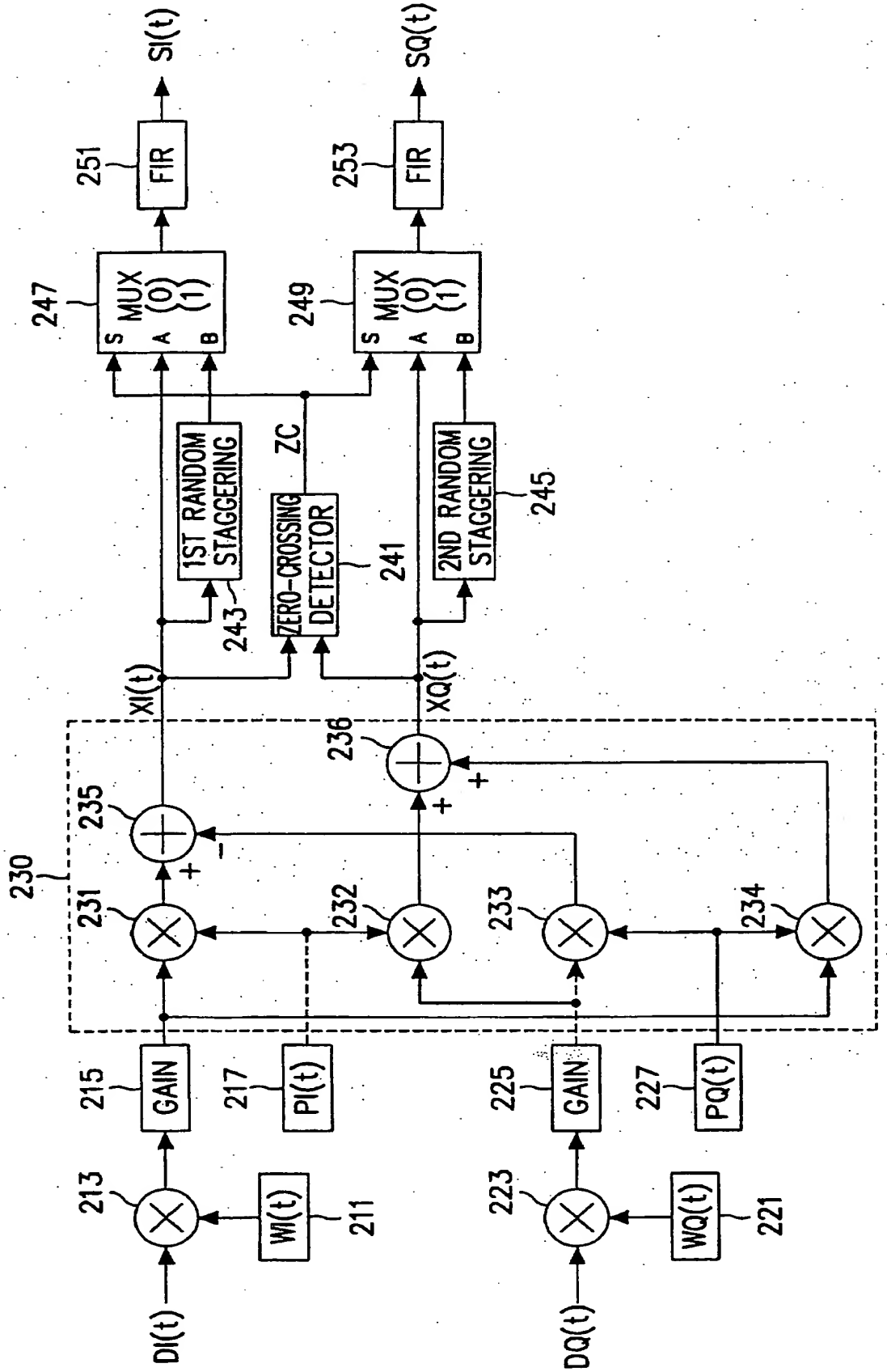
DI(t)
DQ(t)
213
223
WI(t)
211
WQ(t)
221
215
225
GAIN
GAIN
217
227
PI(t)
PQ(t)
230
231
232
233
234
235
236
+
-
+
+
XI(t)
XQ(t)
243
1ST RANDOM STAGGERING
ZERO-CROSSING DETECTOR
241
ZC
2ND RANDOM STAGGERING
245
247
249
MUX
S
A
B
0
1
251
253
FIR
FIR
SI(t)
SQ(t)

FIG. 2

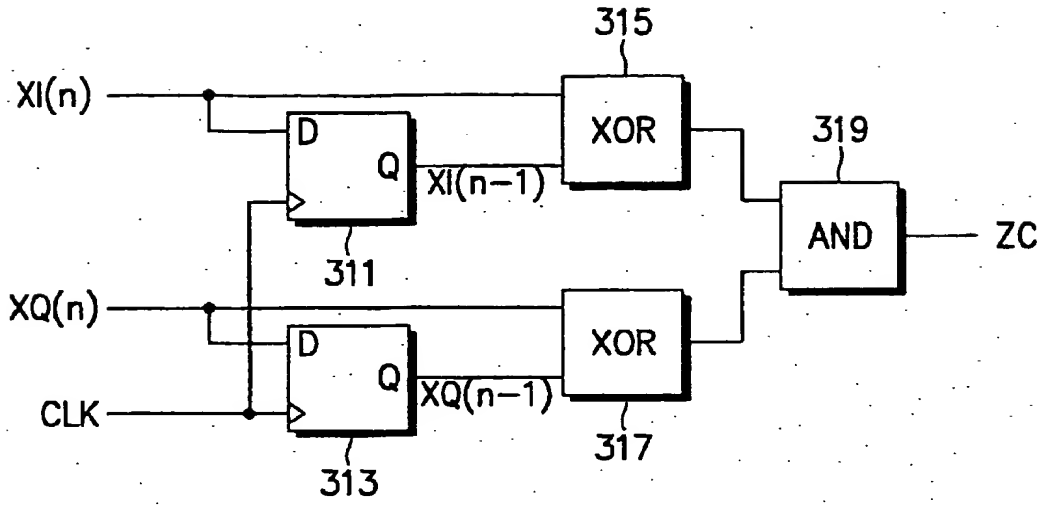
315
XI(n)
D
Q
XOR
319
XI(n-1)
AND
ZC
311
XQ(n)
D
Q
XOR
CLK
XQ(n-1)
317
313

FIG. 3

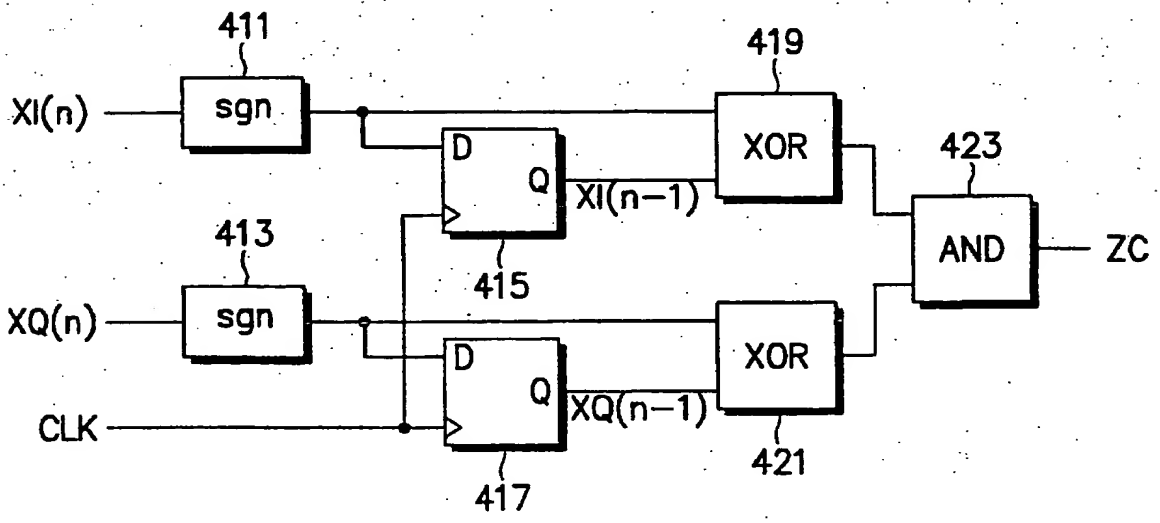
411
419
XI(n)
sgn
D
Q
XOR
423
XI(n-1)
AND
ZC
413
415
XQ(n)
sgn
D
Q
XOR
CLK
XQ(n-1)
421
417

FIG. 4

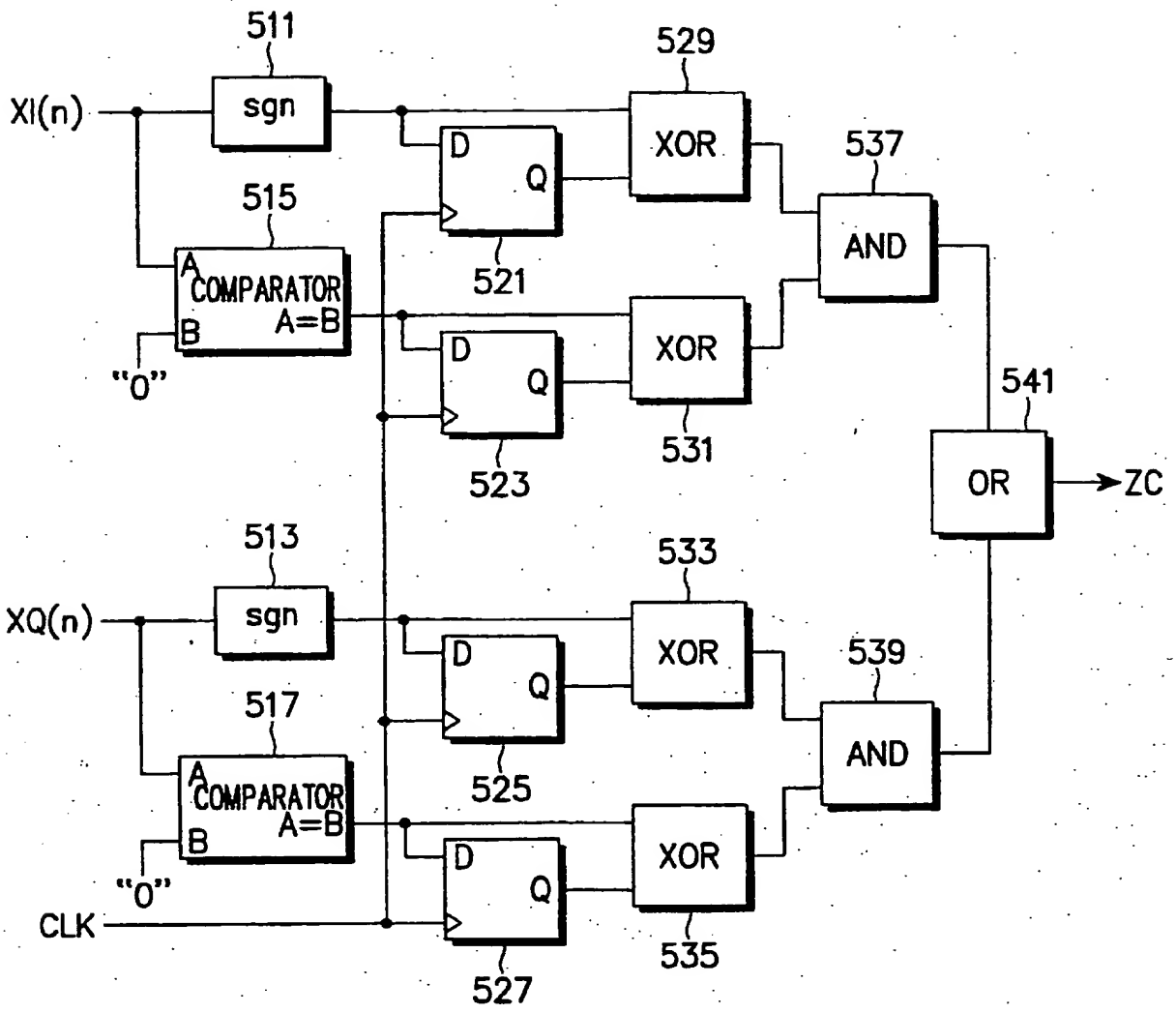
511
529
XI(n)
sgn
D
Q
XOR
537
515
AND
A
COMPARATOR
A=B
B
521
"0"
D
Q
XOR
541
523
531
OR
ZC
513
533
XQ(n)
sgn
D
Q
XOR
539
517
AND
A
COMPARATOR
A=B
B
525
"0"
CLK
D
Q
XOR
535
527

FIG. 5

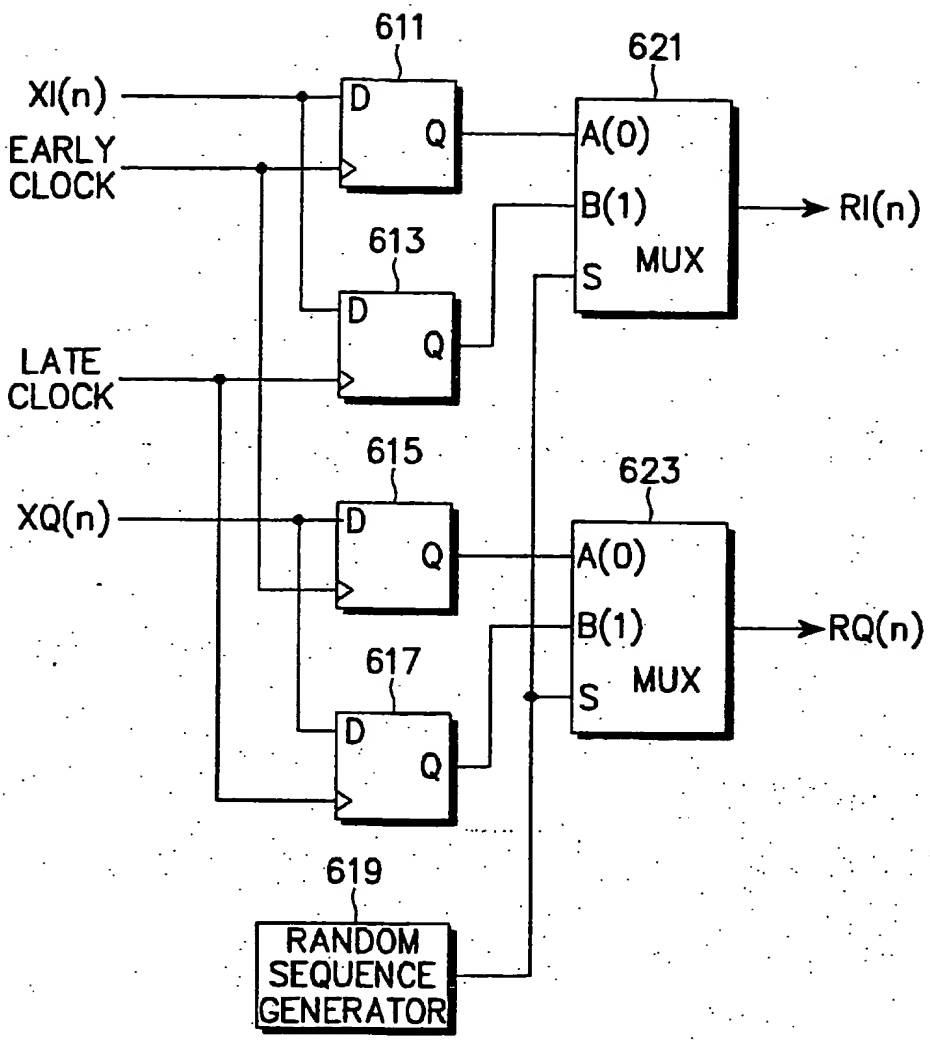
611
621
XI(n)
EARLY CLOCK
D
Q
A(0)
B(1)
S
MUX
RI(n)
613
LATE CLOCK
615
623
XQ(n)
RQ(n)
617
619
RANDOM SEQUENCE GENERATOR

FIG. 6

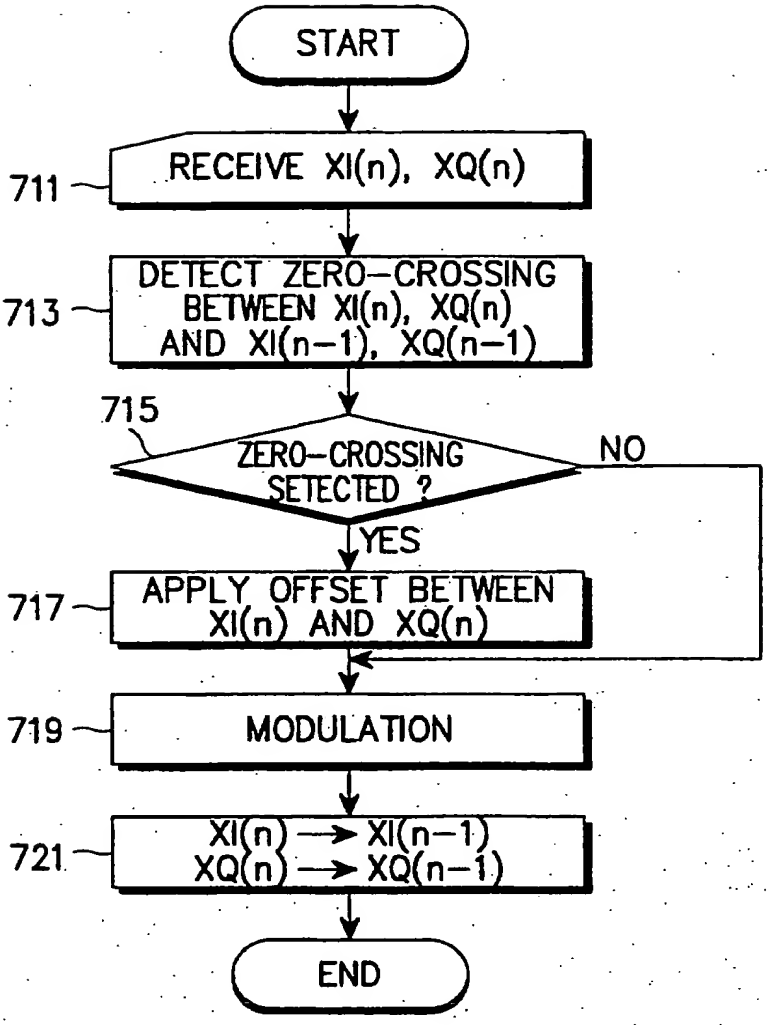
START
711
RECEIVE XI(n), XQ(n)
713
DETECT ZERO-CROSSING BETWEEN XI(n), XQ(n) AND XI(n-1), XQ(n-1)
715
ZERO-CROSSING SETECTED ?
NO
YES
717
APPLY OFFSET BETWEEN XI(n) AND XQ(n)
719
MODULATION
721
XI(n) → XI(n-1)
XQ(n) → XQ(n-1)
END

FIG. 7

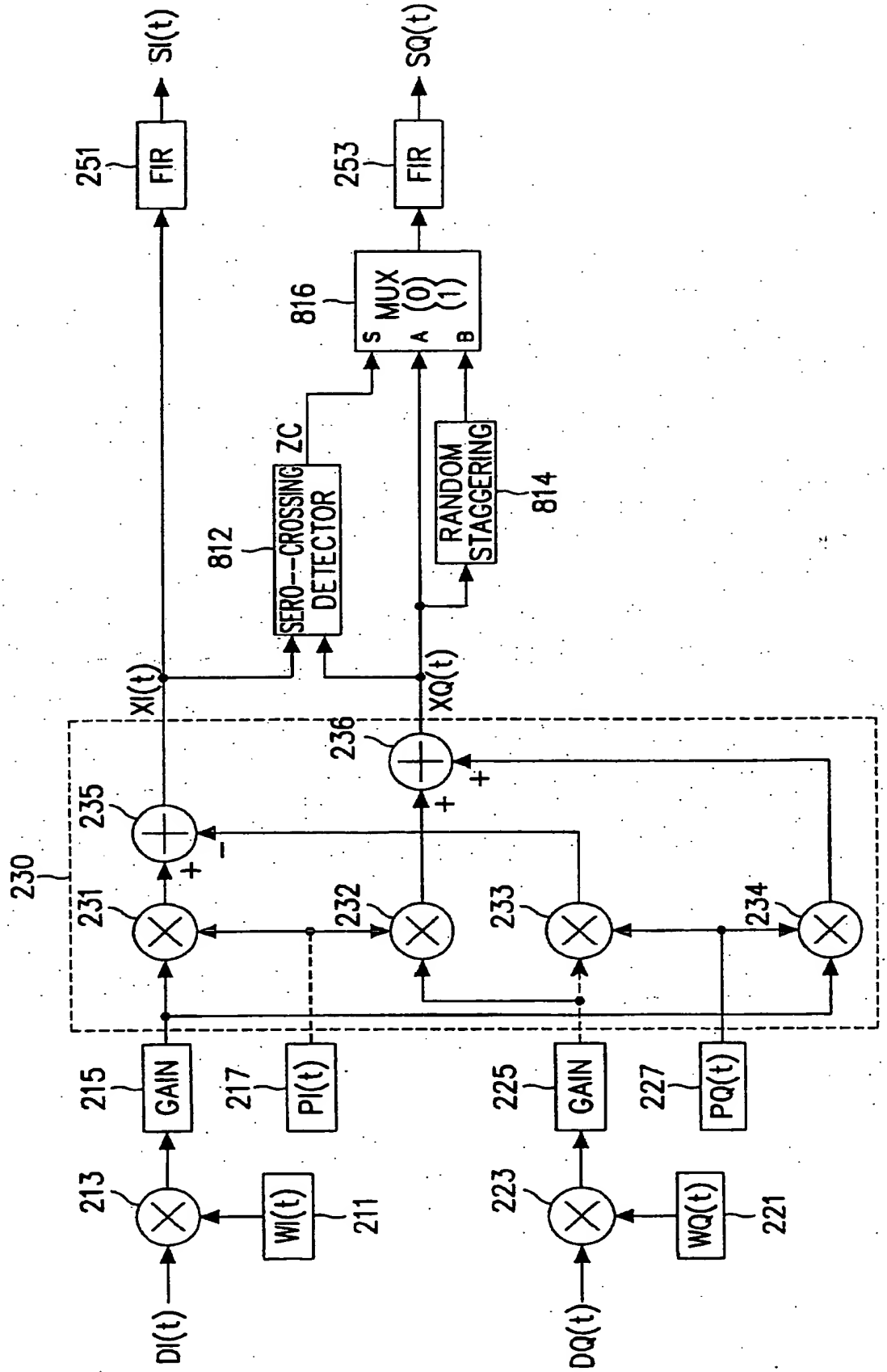
DI(t)
DQ(t)
WI(t)
WQ(t)
211
221
213
223
GAIN
GAIN
215
225
PI(t)
PQ(t)
217
227
230
231
232
233
234
235
236
XI(t)
XQ(t)
ZC
ZERO-CROSSING DETECTOR
812
RANDOM STAGGERING
814
MUX
816
S
A
B
FIR
FIR
251
253
SI(t)
SQ(t)

FIG. 8

MODULATION APPARATUS AND METHOD USING ZERO-CROSSING DETECTION

The present invention relates to a spread spectrum apparatus for a CDMA communication system, and in particular, to an apparatus and method for maintaining orthogonality between channel signals using zero-crossing detection.

Figure 1 illustrates a structure of a spread spectrum apparatus for a conventional OQPSK (Offset Quadrature Phase Shift Keying) DS/CDMA (Direct Sequence/Code Division Multiple Access) communication system.

Referring to figure 1, a multiplier 105 multiplies I-channel (or I-arm) input data DI(t) by an orthogonal code WI(t) to modulate orthogonally the I-channel input data DI(t), and a multiplier 106 multiplies Q-channel (or Q-arm) input data DQ(t) by an orthogonal code WQ(t) to modulate orthogonally the Q-channel input data DQ(t). The orthogonally modulated I- and Q-channel signals are gain controlled in gain controllers 107 and 108, respectively, and then applied to a spreader.

The spreader consists of multipliers 111-114. The multiplier 111 multiplies an output of the gain controller 107 by an I-channel spreading sequence PI(t). The multiplier 112 multiplies an output of the gain controller 108 by the I-channel spreading sequence PI(t). The multiplier 113 multiplies an output of the gain controller 108 by a Q-channel spreading sequence PQ(t) and the multiplier 114 multiplies an output of

the gain controller 107 by the Q-channel spreading sequence PQ(t). A subtracter 115 subtracts an output of the multiplier 113 from an output of the multiplier 111 to generate an I-channel spread signal XI(t), and an adder 116 adds an output of the multiplier 112 to an output of the multiplier 114 to generate a Q-channel spread signal XQ(t). That is, this spreader generates a difference between the signals output from the multipliers 111 and 113 as the I-channel signal XI(t), and a sum of the signals output from the multipliers 112 and 114 as the Q-channel signal XQ(t).

Thereafter, the OQPSK DS/CDMA system delays the Q-channel spread signal XQ(t) by 1/2 chip using a delay 119 prior to filtering the spread signals XI(t) and XQ(t) through FIR (Finite Impulse Response) filters 120 and 121. That is, the I-channel spread signal XI(t) is converted to an I-channel transmission signal SI(t) through the FIR filter 120, and the Q-channel spread signal XQ(t) is delayed by 1/2 chip through the delay 119 and then converted to a Q-channel transmission signal SQ(t) through the FIR filter 121.

As described above, the conventional spread spectrum apparatus delays the Q-channel spread signal XQ(t) by 1/2 chip to prevent zero-crossing of the spread signals XI(t) and XQ(t), thereby avoiding zero-crossing of the transmission signals SI(t) and SQ(t). By avoiding the zero-crossing, the FIR filtered signals have a reduced regrowth of the sidelobe, after being amplified by a non-linear circuit such as a power amplifier at a

following stage.

The CDMA system modulates the user channel using the orthogonal code. In this case, the time and phase of the one channel signal should coincide with that of the other channel signal to maintain the orthogonality between the two channel signals. Accordingly, unlike the QPSK DS/CDMA system, the OQPSK DS/CDMA system shown in figure 1 cannot maintain the orthogonality between the I-channel signal XI(t) and the Q-channel signal XQ(t), which causes a phase error. That is, when an output signal of the OQPSK DS/CDMA system is demodulated at the receiver, the orthogonality between the I-channel signal and Q-channel signal is not maintained accurately even though there is no channel noises. This causes the phase error due to the interference between the channels, resulting in a performance degradation of the system.

It is an object of the present invention to at least mitigate some of the problems associated with the prior art.

Accordingly, the present invention provides modulation apparatus comprising

a zero-crossing detector for determining whether zero-crossing occurs for a first signal and a second signal;

means for outputting the first and second signals so that one signal is delayed with respect to the other as first and second channel signals when the zero-crossing has been detected or the first and second signals as the first and second channel signals when the zero-crossing has not been detected.

Further, an aspect of the present invention provides modulation apparatus comprising

a zero-crossing detector for determining whether zero-crossing occurs for a first signal and a second signal;

means for outputting the first and second signals so that one signal is delayed with respect to the other as first and second channel signals when the zero-crossing has been detected or the first and second signals as the first and second channel signals when the zero-crossing has not been detected.

Advantageously, embodiments of the present invention to provide a spread spectrum apparatus and method capable of maintaining an orthogonality between transmission signals in a CDMA communication system.

Further, embodiments of the present invention provide an apparatus and method capable of avoiding zero-crossing while maintaining an orthogonality by determining whether or not zero-crossing occurs, outputting spread spectrum signals as they are when zero-crossing does not occur and randomly delaying the spread spectrum signals when the zero-crossing occurs in a CDMA communication system.

An embodiment provides a spread spectrum apparatus for a CDMA communication system. In the spread spectrum apparatus, a spreader combines first and second input signals with corresponding PN sequences to generate first and second spread signals. A zero-crossing detector determines whether zero-

crossing occurs between the first spread signal and the second spread signal, to generate a zero-crossing detection signal. A first delay staggers the first spread signal in a first direction and a second delay for staggers the second spread signal in a second direction. A first selector selects one of the first spread signal and a first staggered signal output from the first delay in response to the zero-crossing detection signal, and a second selector selects one of the second spread signal and a second staggered signal output from the second delay in response to the zero-crossing detection signal. The first and second staggered signals are selected when the zero-crossing occurs, and the first and second spread signals are selected when the zero-crossing does not occur, thereby maintaining orthogonality of transmission signals. In an embodiment, the first channel is an in-phase channel and the second channel is a quadrature phase channel.

Preferably, the first delay shifts the first spread signal in a first, preferably positive, direction by a preset chip or fraction of a chip and the second delay shifts the second spread signal in a second, preferably negative, direction by a preset chip or a fraction of a chip. For example, the first delay shifts the first spread signal by +1/4 chip and the second delay shifts the second spread signal by -1/4 chip.

Embodiments of the present invention will now be described by way of example only with reference to the accompanying drawing in which:

figure 1 is a diagram illustrating a spread spectrum

apparatus of a conventional CDMA communication system;

figure 2 is a diagram illustrating a spread spectrum apparatus of a CDMA communication system according to an embodiment of the present invention;

figure 3 is a diagram illustrating a zero-crossing detector (241) of figure 2 according to a first embodiment of the present invention;

figure 4 is a diagram illustrating a zero-crossing detector (241) of figure 2 according to a second embodiment of the present invention;

figure 5 is a diagram illustrating a zero-crossing detector (241) of figure 2 according to a third embodiment of the present invention;

figure 6 is a diagram illustrating a random staggering part (243 or 245) of figure 2 according to an embodiment of the present invention;

figure 7 is a flowchart illustrating a procedure for controlling an output of the spread signals according to whether a zero-crossing occurs or not in the spread spectrum apparatus of a CDMA communication system according to the present invention; and

figure 8 is a diagram illustrating a spread spectrum apparatus according to another embodiment of the present invention.

An OQPSK DS/CDMA system according to the present invention optimally maintains orthogonality between an I-channel signal and a Q-channel signal to minimize the phase error and avoid

zero-crossing, thereby preventing regrowth of the sidelobe. To this end, the exemplary embodiment determines whether or not zero-crossing occurs, to output an I-channel spread signal and a Q-channel spread signal, as they are, when the zero-crossing does not occur and randomly staggering the I-channel signal and the Q-channel spread signal when the zero-crossing is detected, thereby avoiding the zero-crossing and maintaining the orthogonality in the output signal.

A term "delay" used in the specification refers to both retard and advance of a signal, and a term "random staggering" has also the same meaning. Here, retarding or advancing a signal means shifting a signal in a positive or negative direction on a time axis. In addition, a "random staggering part" used in the embodiment has the same function as a normal delay.

Figure 2 illustrates a spread spectrum apparatus for an OQPSK DS/CDMA system according to an embodiment of the present invention. In the figure, orthogonal code generators 211 and 221 generate an I-channel orthogonal code WI(t) and a Q-channel orthogonal code WQ(t), respectively. In the embodiment, Walsh codes are used for the orthogonal codes. A multiplier 213 multiplies an I-channel input signal DI(t) by the orthogonal code WI(t) and outputs an orthogonally modulated signal DI(t)*WI(t). A multiplier 223 multiplies a Q-channel input signal DQ(t) by the orthogonal code WQ(t) and outputs an orthogonally modulated signal DQ(t)*WQ(t). The multipliers 213 and 223 perform orthogonal modulation. A gain controller 215

controls a gain of the orthogonally modulated I-channel signal output from the multiplier 213. A gain controller 225 controls a gain of the orthogonally modulated Q-channel signal output from the multiplier 223.

PN (Pseudo-random Noise) sequence generators 217 and 227 generate an I-channel PN sequence PI(t) and a Q-channel PN sequence PQ(t), respectively. A spreader 230 multiplies the orthogonally modulated I- and Q-channel signals output from the gain controllers 215 and 225 by the PN sequences PI(t) and PQ(t), to spread the orthogonally modulated I- and Q-channel signals. In the spreader 230, a multiplier 231 multiplies the orthogonally modulated I-channel signal DI(t)*WI(t) output from the gain controller 215 by the PN sequence PI(t) and outputs a signal DI(t)*WI(t)*PI(t). A multiplier 232 multiplies the orthogonally modulated Q-channel signal DQ(t)*WQ(t) output from the gain controller 225 by the PN sequence PI(t) and outputs a signal DQ(t)*WQ(t)*PI(t). A multiplier 233 multiplies the orthogonally modulated Q-channel signal DQ(t)*WQ(t) output from the gain controller 225 by the PN sequence PQ(t) and outputs a signal DQ(t)*WQ(t)*PQ(t). A multiplier 234 multiplies the orthogonally modulated I-channel signal DI(t)*WI(t) by the PN sequence PQ(t) and outputs a signal DI(t)*WI(t)*PQ(t). A subtracter 235 subtracts an output of the multiplier 233 from an output of the multiplier 231 and outputs an I-channel spread signal XI(t). Here, XI(t) = DI(t)*WI(t)*PI(t)-DQ(t)*WQ(t)*PQ(t). An adder 236 adds an output of the multiplier 232 to an output of the multiplier 234 and outputs a Q-channel spread signal

XQ(t). Here, XQ(t) = DQ(t)*WQ(t)*PI(t)+DI(t)*WI(t)*PQ(t).

A zero-crossing detector 241 receives the spread signals XI(t) and XQ(t) and determines whether a zero-crossing occurs for both of the two signals, to generate a zero-crossing detection signal ZC according to the determination. A first random staggering part 243 delays (i.e., retards or advances) the I-channel spread signal XI(t) by a given chip unit. A second random staggering part 245 delays the Q-channel spread signal XQ(t) by the given chip unit. A selector 247 has a first input node A receiving the I-channel spread signal XI(t), a second input node B receiving an output of the first random staggering part 243 and a select node S receiving the zero-crossing detection signal ZC output from the zero-crossing detector 241. The selector 247 selects the I-channel spread signal XI(t) when the zero-crossing detection signal ZC represents nonoccurrence of the zero-crossing, and selects the output of the first random staggering part 243 when the zero-crossing detection signal ZC represents occurrence of the zero-crossing. A selector 249 has a first input node A receiving the Q-channel spread signal XQ(t), a second input node B receiving an output of the second random staggering part 245 and a select node S receiving the zero-crossing detection signal ZC output from the zero-crossing detector 241. The selector 249 selects the Q-channel spread signal XQ(t) when the zero-crossing detection signal ZC represents nonoccurrence of the zero-crossing, and selects the output of the second random staggering part 245 when the zero-crossing detection signal ZC represents occurrence of the zero-

crossing.

An FIR filter 251 FIR filters an output of the selector 247 and outputs a transmission signal SI(t). An FIR filter 253 FIR filters an output of the selector 249 and outputs a transmission signal SQ(t).

In operation, the multiplier 213 multiplies the I-channel input signal DI(t) by the orthogonal code WI(t) to modulate orthogonally the I-channel input signal DI(t), and the multiplier 223 multiplies the Q-channel input signal DQ(t) by the orthogonal code WQ(t) to modulate orthogonally the Q-channel input signal DQ(t). The orthogonally modulated I- and Q-channel signals are gain controlled in the gain controllers 215 and 225, respectively, and then spread into the spread signals XI(t) and XQ(t) in the spreader 230.

For generating the spread signals XI(t) and XQ(t), the multiplier 231 multiplies the orthogonally modulated I-channel signal output from the gain controller 215 by the PN sequence PI(t) to generate a spread signal, and the multiplier 233 multiplies the orthogonally modulated Q-channel signal output from the gain controller 225 by the PN sequence PQ(t) to generate a spread signal. The subtracter 235 then calculates the difference between the spread signals output from the multipliers 231 and 233 and outputs the difference as the I-channel spread signal XI(t). Also, the multiplier 232 multiplies the orthogonally modulated Q-channel signal output from the gain

controller 225 by the PN sequence PI(t) to generate a spread signal, and a multiplier 234 multiplies the orthogonally modulated I-channel signal output from the gain controller 215 by the PN sequence PQ(t) to generate a spread signal. The adder 236 then adds the spread signals output from the multipliers 232 and 234 to output the Q-channel spread signal XQ(t).

The OQPSK DS/CDMA system according to the present invention detects the zero-crossing of the spread signals XI(t) and XQ(t) prior to FIR filtering them, and performs OQPSK modulation when the zero-crossing is detected. That is, when the zero-crossing occurs for both of the spread signals XI(t) and XQ(t), the DS/CDMA system performs OQPSK modulation to maintain the 1/2 chip offset between the I-channel signal XI(t) and the Q-channel signal XQ(t), thereby preventing substantially simultaneous zero-crossing between the I-channel transmission signal SI(t) and the Q-channel transmission signal SQ(t). However, when the zero-crossing does not occur for both of the spread signals XI(t) and XQ(t), the DS/CDMA system performs QPSK modulation to maintain the orthogonality between the I-channel signal XI(t) and the Q-channel signal XQ(t), thereby minimizing the phase error.

Here, the zero-crossing detector 241 determines whether or not the zero-crossing occurs for both of the spread signals XI(t) and XQ(t), and generates the zero-crossing detection signal ZC=0 when the zero-crossing does not occur. As a result, the system serves as the QPSK DS/CDMA system. In this case, the

selector 247 selects the spread signal XI(t) and the FIR filter 251 filters the selected spread signal XI(t) to output the transmission signal SI(t). Likewise, the selector 249 selects the spread signal XQ(t) and the FIR filter 253 filters the selected spread signal XQ(t) to output the transmission signal SQ(t).

Figures 3 to 5 illustrate the zero-crossing detector 241 according to different embodiments of the present invention. Figure 3 shows the zero-crossing detector for the case where the spread signals XI(t) and XQ(t) have binary values. Figure 4 shows the zero-crossing detector for the case where the spread signals XI(t) and XQ(t) have multi-level values. Figure 5 shows the zero-crossing detector for the case where the spread signals XI(t) and XQ(t) have multi-level values and one of the spread signals has a zero value. Such a zero-crossing detector 214 determines whether or not the spread signals XI(t) and XQ(t) cross the zero point or not, to output ZC=1 when they cross the zero point together and output ZC=0 when they do not cross the zero point.

Referring to figure 3, when the spread signals XI(t) and XQ(t) have the binary values, the zero-crossing detector 241 detects the case where the (n-1)th spread signals XI(n-1) and XQ(n-1) and the nth spread signals XI(n) and XQ(n) change their levels simultaneously. That is, a flip-flop 311 delays the signal XI(n) by one clock period to output the signal XI(n-1) and a flip-flop 313 delays the signal XQ(t) by one clock period

to output the signal XQ(n-1). An exclusive OR gate 315 exclusively ORs the signal XI(n) and the signal XI(n-1), and an exclusive OR gate 317 exclusives ORs the signal XQ(n) and the signal XQ(n-1). An AND gate 319 ANDs outputs of the exclusive OR gates 315 and 317 to output the zero-crossing detection signal ZC.

The zero-crossing detector 241 of figure 3 detects the zero-crossing and outputs the zero-crossing detection signal ZC=1, when XI(n)=1 and XQ(n)=1 for XI(n-1)=0 and XQ(n-1)=0, when XI(n)=1 and XQ(n)=0 for XI(n-1)=0 and XQ(n-1)=1, when XI(n)=0 and XQ(n)=1 for XI(n-1)=1 and XQ(n-1)=0, or when XI(n)=0 and XQ(n)=0 for XI(n-1)=1 and XQ(n-1)=1. Otherwise, the zero-crossing detector 241 outputs the zero-crossing detection signal ZC=0.

Next, referring to figure 4, when the signal XI(t) and the signal XQ(t) are multi-level signals, the zero-crossing detector 241 detects the case where the (n-1)th signals XI(n-1) and XQ(n-1) and the nth signals XI(n) and XQ(n) change their signs simultaneously. Sign detectors 411 and 413 detect the most significant bits (MSBs) of the signals XI(n) and XQ(n) and output them as sign bits. A flip-flop 415 delays the sign bit of the signal XI(n) by one clock period to output a sign bit of the signal XI(n-1), and a flip-flop 417 delays the sign bit of the signal XQ(n) by one clock period to output a sign bit of the signal XQ(n-1). An exclusive OR gate 419 exclusively ORs the sign bits of the signals XI(n) and XI(n-1), and an exclusive OR

gate 421 exclusively ORs the sign bits of the signals XQ(n) and XQ(n-1). An AND gate 423 ANDs outputs of the exclusive OR gates 419 and 421 to output the zero-crossing detection signal ZC.

Accordingly, the zero-crossing detector of figure 4 detects the zero-crossing and outputs the zero-crossing detection signal ZC=1, when sgn[XI(n),XQ(n)]= -,- for sgn[XI(n-1),XQ(n-1)]=+,+, when sgn[XI(n),XQ(n)]= -,+ for sgn[XI(n-1),XQ(n-1)]=+,-, when sgn[XI(n),XQ(n)]=+,- for sgn[XI(n-1),XQ(n-1)]= -,+, or when sgn[XI(n),XQ(n)]=+,+ for sgn[XI(n-1),XQ(n-1)]= -,-. Here, sgn(X,Y) corresponds to an operation for taking the signs of the signals "X" and "Y". Otherwise, the zero-crossing detector 241 outputs the zero-crossing detection signal ZC=0. In most cases, the sign bit detectors 411 and 413 take the most significant bit to detect the sign bit.

Further, referring to figure 5, when the spread signals XI(t) and XQ(t) are multi-level signals and one of the signals has the zero value, the zero-crossing detector 241 detects the case where the (n-1)th signal XI(n-1) or XQ(n-1) having a non-zero value changes its sign at the nth signal XI(n) or XQ(n).

A sign detector 511 detects the most significant bit of the spread signal XI(n) and output the detected bit as a sign bit. A comparator 515 compares the spread signal XI(n) with a signal of value "0". A flip-flop 521 delays the sign bit of the spread signal XI(n) by one clock period to output a sign bit of the signal XI(n-1). A flip-flop 523 delays an output of the

comparator 515 by one clock period. An exclusive OR gate 529 exclusively ORs the sign bits of the spread signals XI(n) and XI(n-1). An exclusive OR gate 531 exclusively ORs an output of the comparator 515 and an output of the flip-flop 523, and an AND gate 537 ANDs outputs of the exclusive OR gates 529 and 531.

A sign detector 513 detects the most significant bit of the spread signal XQ(n) and outputs the detected bit as a sign bit. A comparator 517 compares the spread signal XQ(n) with a signal of value "0". A flip-flop 525 delays the sign bit of the spread signal XQ(n) by one clock period to output a sign bit of the signal XQ(n-1). A flip-flop 527 delays an output of the comparator 517 by one clock period. An exclusive OR gate 533 exclusively ORs the sign bits of the spread signals XQ(n) and XQ(n-1). An exclusive OR gate 535 exclusively ORs an output of the comparator 517 and an output of the flip-flop 527, and an AND gate 539 ANDs outputs of the exclusive OR gates 533 and 535.

An OR gate 541 ORs outputs of the AND gates 537 and 539 to output the zero-crossing detection signal ZC.

Accordingly, the zero-crossing detector 241 of figure 5 detects the zero-crossing and outputs the zero-crossing detection signal ZC=1, when XI(n)=0 and sgn[XQ(n)]= - for XI(n-1)=0 and sgn[XQ(n-1)]=+, when XI(n)=0 and sgn[XQ(n)]=+ for XI(n-1)=0 and sgn[XQ(n-1)]= -, when sgn[XI(n)]= - and XQ(n)=0 for sgn[XI(n-1)]=+ and XQ(n-1)=0, or when sgn[XI(n)]=+ and XQ(n)=0 for sgn[XI(n-1)]= - and XQ(n-1)=0. Here, sgn(X) corresponds to

an operation for taking the sign of the signal "X". Otherwise, the zero-crossing detector 241 outputs the zero-crossing detection signal ZC=0. In most cases, the sign detectors 511 and 513 take the most significant bit to detect the sign bit.

Moreover, in addition to the structures shown in FIGs. 3 to 5, it is also possible to construct a similar zero-crossing detector in the event where the spread signals XI(t) and XQ(t) undergo the conceptual zero-crossing.

The zero-crossing detector 241 determines whether or not the zero-crossing occurs for both of the spread signals XI(t) and XQ(t) and generates the zero-crossing detection signal ZC=1 when occurrence of the zero-crossing is detected. When ZC=1, the system serves as the OQPSK DS/CDMA system. In this case, the selector 247 selects the spread signal XI(t) which is retarded or advanced by the chip unit in the first random staggering part 243, and the FIR filter 251 filters the output of the first random staggering part 243 to output the transmission signal SI(t). Further, a selector 249 selects the spread signal XQ(t) which is retarded or advanced by the chip unit in the second random staggering part 245, and the FIR filter 253 filters the output of the second random staggering part 245 to output the transmission signal SQ(t).

Assuming that the I-channel signal and the Q-channel signal should have the 1/2 chip phase difference, the first random staggering part 243 and the second random staggering part

245 can be realized in several methods as follows:

In a first method, a random number is generated. When the generated random number is a positive number (+), and the spread signal XI(t) is delayed by +1/4 chip and the spread signal XQ(t) is delayed by -1/4 chip, thus maintaining the 1/2 chip difference between the spread signals XI(t) and XQ(t). However, when the generated random number is a negative number (-), the spread signal XI(t) is delayed by -1/4 chip and the spread signal XQ(t) is delayed by +1/4 chip, thus maintaining the 1/2 chip difference between the spread signals XI(t) and XQ(t).

In a second method, a random number is generated. When the generated random number is a positive number (+), the spread signal XI(t) is delayed by -1/4 chip and the spread signal XQ(t) is delayed by +1/4 chip, thus maintaining the 1/2 chip difference between the spread signals XI(t) and XQ(t). However, when the generated random number is a negative number (-), the spread signal XI(t) is delayed by +1/4 chip and the spread signal XQ(t) is delayed by -1/4 chip, thus maintaining the 1/2 chip difference between the spread signals XI(t) and XQ(t).

Figure 6 illustrates the structure of the random staggering part 243 (or 245). Referring to figure 6, to maintain the 1/2 chip difference between the I-channel signal and the Q-channel signal, an early clock CK1 is advanced by +1/4 chip with respect to a reference clock and a late clock CK2 is retarded by -1/4 chip with respect to the reference clock. A random sequence

generator 619 generates random sequences. Here, the random sequence generator 619 can be a PN (Pseudo-random Noise) sequence generator. In the figure, flip-flops 611 and 613 and a selector 621 constitute the first random staggering part 243, and flip-flops 615 and 617 and a selector 623 constitute the second random staggering part 245.

In operation, a signal RI(n) is delayed by +/- 1/4 chip with respect to the spread signal XI(n) at a reference time and a signal RQ(n) is delayed by -/+ 1/4 chip with respect to the spread signal XQ(n) at the reference time, according to an output of the random sequence generator 619. Accordingly, the signals RI(n) and RQ(n) also have the 1/2 chip difference. Although the zero-crossing occurs for the signals XI(n) and XQ(n), the 1/2 chip difference between the signals RI(n) and RQ(n) is maintained, avoiding the zero-crossing.

Figure 7 is a flowchart illustrating a procedure for determining whether or not the zero-crossing occurs for both of the two different channel signals in the CDMA communication system according to the present invention. Referring to figure 7, as the new I- and Q-channel signals XI(n) and XQ(n) are received in step 711, the current I- and Q-channel signals XI(n) and XQ(n) and the previous I- and Q-channel signals XI(n-1) and XQ(n-1) are analyzed in step 713. It is determined in step 715 whether the zero-crossing has occurred between I-channel signals XI(n) and XI(n-1) and whether or not zero-crossing has occurred between the Q-channel signals XQ(n) and XQ(n-1), in the manner

shown in figures 3, 4 and 5. When it is determined in step 715 that the zero-crossing has not occurred between the I-channel signals and the Q-channel signals, the current input signals XI(n) and XQ(n) are output as the transmission signals without offset, in step 719. After modulating the input signals without offset, the signals XI(n) and XQ(n) are stored as signals XI(n-1) and XQ(n-1), respectively, preparing for the next state.

However, when the zero-crossing has occurred for the I-channel signal XI(n) and the Q-channel signal XQ(n) in step 715, the I-channel signal XI(n) and the Q-channel signal XQ(n) are so controlled as to have the offset in the chip unit. For the offset, it is possible to provide a preset offset by staggering the signals XI(n) and XQ(n) in different directions or by staggering one of the signals XI(n) and XQ(n) by a preset value. In addition, it is possible to provide the desired offset by staggering the signals XI(n) and XQ(n) by a fixed value or a random value. When the signals XI(n) and XQ(n) are so staggered as to have the offset value, there does not occur the zero-crossing between the signals XI(n) and XQ(n). Then, in step 719, the signals XI(n) and XQ(n), which are offset by a predetermined value, are modulated and output as the transmission signals. After offsetting the input signals to modulate them, the signals XI(n) and XQ(n) are stored as signals XI(n-1) and XQ(n-1), respectively, preparing for the next state.

Accordingly, the spread spectrum apparatus according to the present invention includes a scheme for detecting zero-

crossing of the I (In-phase) channel signal and the Q (Quadrature-phase) channel signal, to provide, when the zero-crossing occurs, a difference (or offset) between the I-channel signal and the Q-channel signal in order to prevent the I- and Q-channel signals from being changed simultaneously, and to transmit the I- and Q-channel signals, as they are, when the zero-crossing does not occur. Therefore, the embodiment transmits the channel signals, as they are, when the zero-crossing does not occur for the two channel signals, and provides an offset between the I- and Q-channel signals to prevent zero-crossing before transmission, when the zero-crossing is detected. That is, the embodiment detects occurrence of the zero-crossing for the I-channel signal and the Q-channel signal, to provide an offset therebetween before transmission, only when the zero-crossing has been detected.

Here, to provide an offset between the I-channel signal and the Q-channel signal, the embodiment includes the random staggering parts 243 and 244 on the I-channel and the Q-channel, respectively, as shown in figure 2, and delays the corresponding channel signals, for example, by 1/4 chip using the random staggering parts 243 and 245. However, it can be understood that any signal retarding or advancing technique can be used in place of the signal random staggering technique. That is, it is possible to use a technique for fixedly delaying the I-channel signal by +1/4 chip and the Q-channel signal by -1/4 chip, upon detection of the zero-crossing. In addition, when a time T is shorter than one chip time, it is also possible to delay (retard

or advance) the I-channel signal by +T and the Q-channel signal by -T, instead of 1/4 chip.

Moreover, it is also possible to connect the random staggering part to a selected one of the I-channel and the Q-channel, instead of connecting the random staggering parts both to the I-channel and Q-channel. Figure 8 illustrates the spread spectrum apparatus having the random staggering part only on the Q-channel.

Referring to figure 8, the orthogonal code generators 211 and 221 generate the I-channel orthogonal code WI(t) and the Q-channel orthogonal code WQ(t), respectively. In the embodiment, Walsh codes are used for the orthogonal codes. The multiplier 213 multiplies the I-channel input signal DI(t) by the orthogonal code WI(t) and outputs an orthogonally modulated signal DI(t)*WI(t). The multiplier 223 multiplies the Q-channel input signal DQ(t) by the orthogonal code WQ(t) and outputs an orthogonally modulated signal DQ(t)*WQ(t). The multipliers 213 and 223 perform orthogonal modulation. The gain controller 215 controls a gain of the orthogonally modulated I-channel signal output from the multiplier 213. The gain controller 225 controls a gain of the orthogonally modulated Q-channel signal output from the multiplier 223.

PN sequence generators 217 and 227 generate the I-channel PN sequence PI(t) and the Q-channel PN sequence PQ(t), respectively. The spreader 230 multiplies the orthogonally

modulated I- and Q-channel signals output from the gain controllers 215 and 225 by the PN sequences PI(t) and PQ(t), respectively, to spread the orthogonally modulated I- and Q-channel signals. In the spreader 230, the multiplier 231 multiplies the orthogonally modulated I-channel signal DI(t)*WI(t) output from the gain controller 215 by the PN sequence PI(t) and outputs a signal DI(t)*WI(t)*PI(t). The multiplier 232 multiplies the orthogonally modulated Q-channel signal DQ(t)*WQ(t) output from the gain controller 225 by the PN sequence PI(t) and outputs a signal DQ(t)*WQ(t)*PI(t). The multiplier 233 multiplies the orthogonally modulated Q-channel signal DQ(t)*WQ(t) output from the gain controller 225 by the PN sequence PQ(t) and outputs a signal DQ(t)*WQ(t)*PQ(t). The multiplier 234 multiplies the orthogonally modulated I-channel signal DI(t)*WI(t) by the PN sequence PQ(t) and outputs a signal DI(t)*WI(t)*PQ(t). The subtracter 235 subtracts an output of the multiplier 233 from an output of the multiplier 231 and outputs an I-channel spread signal XI(t). Here, XI(t) = DI(t)*WI(t)*PI(t)-DQ(t)*WQ(t)*PQ(t). The adder 236 adds an output of the multiplier 232 to an output of the multiplier 234 an outputs a Q-channel spread signal XQ(t). Here, XQ(t) = DQ(t)*WQ(t)*PI(t)+DI(t)*WI(t)*PQ(t).

A zero-crossing detector 812 receives the spread signals XI(t) and XQ(t) and determines whether the zero-crossing occurs for the two signals, to generate a zero-crossing detection signal ZC according to the determination. The zero-crossing detector 812 may have the same structure and operation as that

shown in figures 3, 4 and 5. A random staggering part 814 retards or advances the Q-channel signal by the chip unit. The random staggering part 814 may have the same structure and operation as that shown in figure 6. Here, the random staggering part 814 can retard or advance the Q-channel signal XQ(t) by the 1/2 chip unit. A selector 816 has a first input node A receiving the Q-channel spread signal XQ(t), a second input node B receiving an output of the random staggering part 812 and a select node S receiving the zero-crossing detection signal ZC output from the zero-crossing detector 812. The selector 816 selects the Q-channel spread signal XQ(t) when the zero-crossing detection signal ZC represents nonoccurrence of the zero-crossing, and selects the output of the second random staggering part 816 when the zero-crossing detection signal ZC represents occurrence of the zero-crossing.

The FIR filter 251 FIR filters an output of the selector 247 and outputs a transmission signal SI(t). The FIR filter 253 FIR filters an output of the selector 249 and outputs a transmission signal SQ(t).

When the zero-crossing occurs, the spread spectrum apparatus of figure 8 delays only the Q-channel signal by the 1/2 chip unit to avoid the zero-crossing. However, when the zero-crossing does not occur, the I-channel signal and the Q-channel signal are transmitted as they are (without delay), in the same manner as described in figure 2. Although figure 8 shows an exemplary structure in which the random staggering part

is connected to the Q-channel, it is also possible to connect the random staggering part to the I-channel.

Although the present invention has been described with reference to the DS/CDMA system which selectively uses QPSK or OQPSK modulation according to the zero-crossing detection, the inventive concept can also be applied to a non-DS/CDMA system which mixedly uses QPSK and OQPSK modulation. In this case, the signals output from the FIR filters 251 and 253 are input as I- and Q-channel signals of the QPSK modulator, respectively.

As described above, the OQPSK DS/CDMA system according to the present invention detects occurrence of the zero-crossing for the spread signals of the I-channel and the Q-channel, uses QPSK modulation to maintain the orthogonality between the channels when the zero-crossing does not occur, and uses OQPSK modulation by random staggering to avoid the zero-crossing between the spread signals when the zero-crossing occurs. Accordingly, it is possible to prevent regrowth of the sidelobe and minimize the phase error due to the non-orthogonality between the I-channel signal and the Q-channel signal, which is a drawback of OQPSK modulation.

While the invention has been shown and described with reference to a certain preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended

claims.

CLAIMS

1. Modulation apparatus comprising

a zero-crossing detector for determining whether zero-crossing occurs for a first signal and a second signal;

means for outputting the first and second signals so that one signal is delayed with respect to the other as first and second channel signals when the zero-crossing has been detected or the first and second signals as the first and second channel signals when the zero-crossing has not been detected.

2. Apparatus as claimed in claim 1, comprising:

a first delay for delaying the first input signal in a first direction by a preset period;

a second delay for delaying the second input signal in a second direction by the preset period; and

a selector for selecting the outputs of the first and second delays as first and second channel signals when the zero-crossing occurs, and selecting the first and second input signals as the first and second channel signals when the zero-crossing does not occur.

3. Apparatus as claimed in claim 2, wherein the first delay shifts the first input signal in a positive direction by the preset period and the second delay shifts the second input signal in a negative direction by the preset period.

4. Apparatus as claimed in claim 2, wherein the first delay shifts the first input signal in a negative direction by the

preset period and the second delay shifts the second input signal in a positive direction by the preset period.

5. Apparatus as claimed in any preceding claim, wherein the first channel is an in-phase channel and the second channel is a quadrature phase channel.

6. Apparatus as claimed in claim 1, comprising:

a delay for shifting the first input signal by a preset period; and

a selector for selecting the output of the delay and the second input signal as first and second channel signals when the zero-crossing occurs, and selecting the first and second input signals as the first and second channel signals when the zero-crossing does not occur.

7. Apparatus as claimed in claim 6, wherein said delay shifts the first input signal in a positive direction by the preset period.

8. Apparatus as claimed in claim 6, wherein said delay shifts the first input signal in a negative direction by the preset period.

9. Apparatus as claimed in any of claims 6 to 8, wherein the first channel is an in-phase channel.

10. Apparatus as claimed in any of claims 6 to 8, wherein the

first channel is a quadrature phase channel.

11. A spread spectrum apparatus for a CDMA (Code Division Multiple Access) communication system, comprising:

a spreader for combining first and second input signals with corresponding PN (Pseudo-random Noise) sequences to generate first and second spread signals;

a zero-crossing detector for determining whether zero-crossing occurs between the first spread signal and the second spread signal, to generate a zero-crossing detection signal;

means for outputting the first and second spread signals so that one signal is delayed with respect to the other as first and second channel signals when the zero-crossing has been detected or the first and second spread signals as the first and second channel signals when the zero-crossing has not been detected.

12. Apparatus as claimed in claim 11, comprising:

a first delay for staggering the first spread signal in a first direction;

a second delay for staggering the second spread signal in a second direction;

a first selector for selecting one of the first spread signal and a first staggered signal output from the first delay in response to the zero-crossing detection signal; and

a second selector for selecting one of the second spread signal and a second staggered signal output from the second delay in response to the zero-crossing detection signal;

whereby the first and second staggered signals are selected when the zero-crossing occurs, and the first and second spread signals are selected when the zero-crossing does not occur, thereby maintaining an orthogonality of transmission signals.

13. Apparatus as claimed in claim 12, wherein the first delay shifts the first spread signal in a positive direction by a preset chip and the second delay shifts the second spread signal in a negative direction by a preset chip.

14. Apparatus as claimed in claim 13, wherein the first delay shifts the first spread signal by +1/4 chip and the second delay shifts the second spread signal by -1/4 chip.

15. Apparatus as claimed in claim 12, wherein the first delay shifts the first spread signal in a negative direction by a preset chip and the second delay shifts the second spread signal in a positive direction by a preset chip.

16. Apparatus as claimed in claim 15, wherein the first delay shifts the first spread signal by -1/4 chip and the second delay shifts the second spread signal by +1/4 chip.

17. Apparatus as claimed in any of claims 12 to 16, wherein the first channel is an in-phase channel and the second channel is a quadrature phase channel.

18. Apparatus as claimed in any preceding claim, wherein the first input signal and the second input signal are respectively a first orthogonally modulated signal and a second orthogonally modulated signal which are combined with corresponding orthogonal codes.

19. Apparatus as claimed in claim 12, comprising:

a delay for staggering the first spread signal; and

a selector for selecting the second spread signal and a staggered signal output from the delay in response to the zero-crossing detection signal;

whereby the first spread signal and the staggered signal are selected when the zero-crossing occurs, and the first and second spread signals are selected when the zero-crossing does not occur, thereby maintaining an orthogonality of transmission signals.

20. Apparatus as claimed in claim 19, wherein the delay shifts the first spread signal in a positive direction by a preset chip.

21. Apparatus as claimed in claim 19, wherein the delay shifts the first spread signal in a negative direction by a preset chip.

22. Apparatus as claimed in either of claims 20 or 21, wherein the delay shifts the first spread signal by 1/2 chip.

23. Apparatus as claimed in claim any of claims 19 to 22, wherein the first channel is an in-phase channel.

24. Apparatus as claimed in any of claims 19 to 22, wherein the first channel is a quadrature phase channel.

25. Apparatus as claimed in any of claims 19 to 24, wherein the first input signal and the second input signal are respectively a first orthogonally modulated signal and a second orthogonally modulated signal which are combined with corresponding orthogonal codes.

26. Apparatus as claimed in preceding claim, further comprising

a modulator for QPSK modulating the first and second channel signals.

27. A method comprising the steps of

determining whether zero-crossing occurs for a first input signal and a second input signal; and

outputting the first and second input signals so that one signal is delayed with respect to the other as first and second channel signals when the zero-crossing has been detected or the first and second input signals as the first and second channel signals when the zero-crossing has not been detected.

28. A method as claimed in claim 27, comprising the steps of

delaying the first input signal in a first direction by a preset period;

delaying the second input signal in a second direction by the preset period; and

selecting the outputs of the first and second delays as first and second channel signals when the zero-crossing occurs, and selecting the first and second input signals as the first and second channel signals when the zero-crossing does not occur.

29. A method as claimed in claim 28, wherein the first delay shifts the first input signal in a positive direction by the preset period and the second delay shifts the second input signal in a negative direction by the preset period.

30. A method as claimed in claim 28, wherein the first delay shifts the first input signal in a negative direction by the preset period and the second delay shifts the second input signal in a positive direction by the preset period.

31. A method as claimed in any of claims 27 to 30, wherein the first channel is an in-phase channel and the second channel is a quadrature phase channel.

32. A method as claimed in claim 27, comprising the steps of

shifting the first input signal by a preset period; and

selecting the output of the delay and the second input signal as first and second channel signals when the zero-crossing occurs, and selecting the first and second input signals as the first and second channel signals when the zero-

crossing does not occur.

33. A method as claimed in claim 32, wherein the step of shifting shifts the first input signal in a positive direction by the preset period.

34. A method as claimed in claim 32, wherein the step of shifting shifts the first input signal in a negative direction by the preset period.

35. A method as claimed in any of claims 32 to 34, wherein the first channel is an in-phase channel.

36. A method as claimed in any of claims 32 to 34, wherein the first channel is a quadrature phase channel.

37. A spread spectrum method for a CDMA (Code Division Multiple Access) communication system, the method comprising the steps of

combining first and second input signals with corresponding PN (Pseudo-random Noise) sequences to generate first and second spread signals;

determining whether zero-crossing occurs between the first spread signal and the second spread signal, to generate a zero-crossing detection signal; and

outputting the first and second spread signals so that one signal is delayed with respect to the other as first and second channel signals when the zero-crossing has been detected or the first and second spread signals as the first and second channel

signals when the zero-crossing has not been detected.

38. A method as claimed in claim 37, comprising the steps of

staggering the first spread signal in a first direction;

staggering the second spread signal in a second direction;

selecting one of the first spread signal and a first staggered signal output from the first delay in response to the zero-crossing detection signal; and

selecting one of the second spread signal and a second staggered signal output from the second delay in response to the zero-crossing detection signal;

whereby the first and second staggered signals are selected when the zero-crossing occurs, and the first and second spread signals are selected when the zero-crossing does not occur, thereby maintaining an orthogonality of transmission signals.

39. A method as claimed in claim 38, wherein the step of staggering the first spread signal shifts the first spread signal in a positive direction by a preset chip and the step of staggering the second spread signal shifts the second spread signal in a negative direction by a preset chip.

40. A method as claimed in claim 39, wherein the step of staggering the first spread signal shifts the first spread signal by +1/4 chip and the step of staggering the second spread signal shifts the second spread signal by -1/4 chip.

41. A method as claimed in claim 38, wherein the step of staggering the first spread signal shifts the first spread signal in a negative direction by a preset chip and the step of staggering the second spread signal shifts the second spread signal in a positive direction by a preset chip.

42. A method as claimed in claim 41, wherein the step of staggering the first spread signal shifts the first spread signal by -1/4 chip and the step of staggering the second spread signal shifts the second spread signal by +1/4 chip.

43. A method as claimed in any of claims 38 to 42, wherein the first channel is an in-phase channel and the second channel is a quadrature phase channel.

44. A method as claimed in any of claims 27 to 43, wherein the first input signal and the second input signal are respectively a first orthogonally modulated signal and a second orthogonally modulated signal which are combined with corresponding orthogonal codes.

45. A method as claimed in claim 27, comprising the steps of

staggering the first spread signal; and

selecting the second spread signal and a staggered signal output from the delay in response to the zero-crossing detection signal;

whereby the first spread signal and the staggered signal are selected when the zero-crossing occurs, and the first and

second spread signals are selected when the zero-crossing does not occur, thereby maintaining an orthogonality of transmission signals.

46. A method as claimed in claim 45, wherein the step of staggering the first spread signal shifts the first spread signal in a positive direction by a preset chip.

47. A method as claimed in claim 45, wherein the step of staggering the first spread signal shifts the first spread signal in a negative direction by a preset chip.

48. A method as claimed in either of claims 46 or 47, wherein the step of staggering shifts the first spread signal by 1/2 chip.

49. A method as claimed in claim any of claims 45 to 48, wherein the first channel is an in-phase channel.

50. A method as claimed in any of claims 45 to 48, wherein the first channel is a quadrature phase channel.

51. A method as claimed in any of claims 45 to 50, wherein the first input signal and the second input signal are respectively a first orthogonally modulated signal and a second orthogonally modulated signal which are combined with corresponding orthogonal codes.

52. A method as claimed in of claims 27 to 51, further comprising

QPSK modulating the first and second channel signals.

53. A communication method substantially as described herein with reference to and/or as illustrated in figures 2 to 8 of the accompanying drawings.

54. Communication apparatus substantially as described herein with reference to and/or as illustrated in figures 2 to 8 of the accompanying drawings.

Application No: GB 9904815.9 **Examiner:** Matthew Nelson
Claims searched: 1-54 **Date of search:** 26 August 1999

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H4P (PABX, PAN, PAPX, PAQ, PDCSL)

Int Cl (Ed.6): H04B 1/707, 7/216; H04J 11/00, 13/02, 13/04; H04L 23/02, 27/00, 27/18, 27/20

Other: Online:- WPI, EPODOC, JAPIO, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0795983 A1	(DEUTSCHE ITT INDUSTRIES) See abstract	
A,E	US 5903555	(WILDAUER et al) See col. 3, line 53 - col. 4, line 50	
A,P	US 5818867	(RASMUSSEN et al) See col. 2, lines 35-60	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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